$$P_{ac} = I_{rms}^2 (r_f + R_L) = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)$$

Rectification efficiency

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 R_L}{(I_m/\sqrt{2})^2 (r_f + R_L)} \times 100\% = \frac{81.2}{1 + r_f/R_L}\%$$

If $r_f << R_L$,

Maximum rectification efficiency, $\eta = 81.2\%$

- **Form factor**
  - Form factor $= \frac{I_{rms}}{I_{dc}}$
  - For half wave rectifier,

$$I_{rms} = \frac{I_m}{2},\ I_{dc} = \frac{I_m}{\pi}$$

$$\text{Form factor} = \frac{I_m/2}{I_m/\pi} = \frac{\pi}{2} = 1.57$$

  - For full wave rectifier,

$$I_{rms} = \frac{I_m}{\sqrt{2}},\ I_{dc} = \frac{2I_m}{\pi}$$

$$\text{Form factor} = \frac{I_m/\sqrt{2}}{2I_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

Illustration 5

~~In a full wave~~ rectifier circuit operating from 50 Hz mains frequency. What is the fundamental frequency in the ripple?

Soln.: 100 Hz.

In full wave rectifier, we get the output for the positive and the negative cycles of input ac Hence, the frequency of the ripple of the output is twice than that of input ac.

Illustration 6

An alternating voltage of 350 V, 60 Hz is applied on a full wave rectifier. The internal resistance of each diode is 200 W. If R_L = 5 kW, then find

(i) the peak value of output current.
(ii) the value of output direct current.
(iii) the output dc power.
(iv) the rms value of output current.
(v) the efficiency of rectifier.
(vi) the value of peak inverse voltage (*P.I.V.*).

Sol. (i) $I_{peak} = I_{rms} \times \sqrt{2} = \frac{V_{rms} \times \sqrt{2}}{(R_L + 2r_p)}$

or $I_0 = \frac{350 \times \sqrt{2}}{(5000 + 400)}$ ~~or I_0~~ $= \frac{350 \times 1.414}{5400} = 0.092\text{A}$

(ii) $I_{DC} = \frac{2I_0}{\pi} = \frac{2 \times 0.092}{3.14} = 0.058$ A

(iii) $P_{DC} = I_{DC}^2 \times R_L = (0.058)^2 \times (5000) \simeq 17$ W

(iv) $I_{rms} = \frac{I_0}{\sqrt{2}} = \frac{0.092}{1.41} = 0.065$ A

(v) Efficiency of rectifier $\eta = \frac{81.6}{1 + \frac{r_p}{R_L}}$

or $\eta = \frac{81.6}{1 + \frac{200}{5000}} = \frac{81.6 \times 25}{26}$ or $\eta = 78\%$.

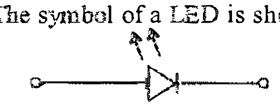
(vi) $P.I.V. = 2E_0$

or $P.I.V. = 2\sqrt{2}\ E_{rms} = 2\sqrt{2} \times 350$

or $P.I.V. \simeq 1000$ V.

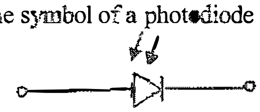
LIGHT EMITTING DIODE (LED)

- It converts electrical energy into light energy.
- It is a heavily doped *p-n* junction which under forward bias emits spontaneous radiation.
- The *I-V* characteristics of a LED is similar to that of Si junction diode. But the threshold voltages are much higher and slightly different for each colour. The reverse breakdown voltages of LEDs are very low, typically around 5 V.
- The semiconductor used for fabrication of visible LEDs must at least have a band gap of 1.8 eV.
- The compound semiconductor gallium arsenide phosphide (GaAsP) is used for making LEDs of different colours.
- GaAs is used for making infrared LED.
- The symbol of a LED is shown in the figure.



PHOTODIODE

- A photodiode is a special type *p-n* junction diode fabricated with a transparent window to allow light to fall on the diode.
- It is operated under reverse bias.
- When it is illuminated with light of photon energy greater than the energy gap of the semiconductor, electron-hole pairs are generated in near depletion region.
- The symbol of a photodiode is shown in the figure below.



SOLAR CELL

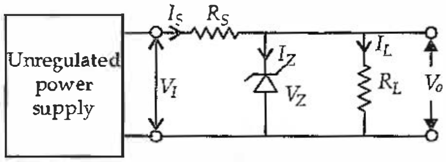
- It converts solar energy into electrical energy.
- A solar cell is basically a *p-n* junction which generates emf when solar radiation falls on the *p-n* junction.
- It works on the same principle (photovoltaic effect) as the photodiode, except that no external bias is applied and the junction area is kept large.

ZENER DIODE

- It was invented by C. Zener. It is designed to operate under reverse bias in the breakdown region and is used as a voltage regulator. The symbol for Zener diode is shown in the figure.

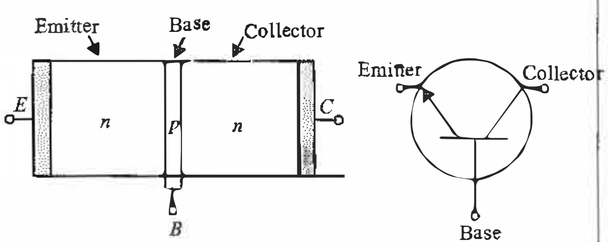
Zener Diode as a Voltage Regulator

- The circuit diagram for zener diode as a voltage regulator is shown in the figure below.

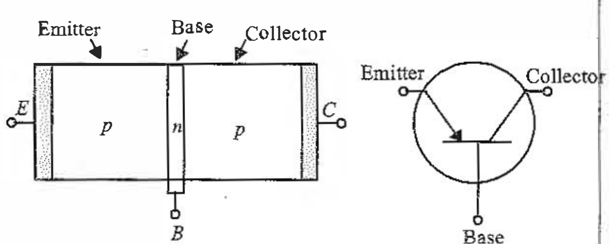


TRANSISTOR: STRUCTURE AND ACTION

- A transistor has three doped regions forming two *p-n* junctions between them. There are two types of transistors, as shown in figure.
  - **n-p-n transistor:** Here two segments of *n*-type semiconductor (emitter and collector) are separated by a segment of *p*-type semiconductor (base).



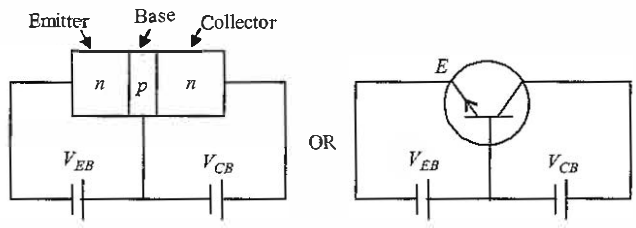
  - **p-n-p transistor:** Here two segments of *p*-type semiconductor (termed as emitter and collector) are separated by a segment of *n*-type semiconductor (termed as base).



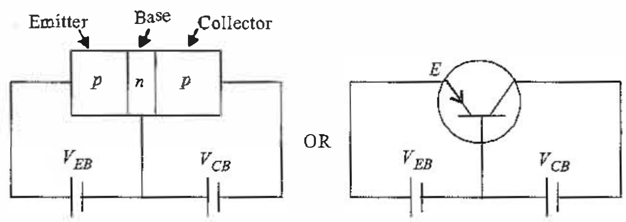
- Every transistor consists of three regions.
  - **Emitter** is the section on one side of transistor, that supplies charge carriers. It is heavily doped and is always kept forward biased with respect to base, so that it can supply a large number of charge carriers to the base.
  - **Collector** is the section on the other side of transistor, that collects the charge carriers. It is moderately doped but large in size and is always kept in reverse bias with respect to base.
  - **Base** is the middle section of transistor, that forms two *p-n* junctions with emitter and collector. It is very thin and lightly doped so as to pass most of the emitter injected charge carriers to the collector.

Circuit Connections of Transistor

- The circuit of a transistor is always joined such as the emitter base circuit is forward biased and collector-base circuit is reversed bias.



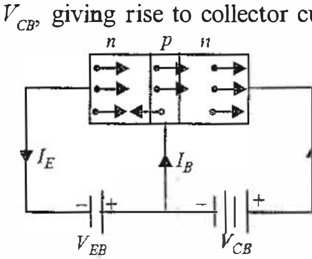
Circuit connection for *npn* transistor



Circuit connection for *pnp* transistor

Action of *n-p-n* Transistor

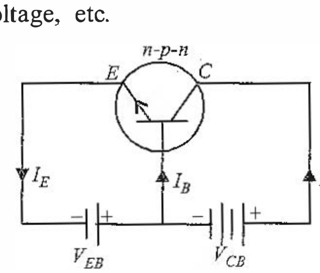
- The forward bias of the emitter-base circuit repels the electrons of emitter towards the base, setting up emitter current I_E. As the base is very thin and lightly doped, a very few electrons ($\approx$ 5%) from the emitter combine with the holes of base, giving rise to base current I_B and the remaining electrons ($\approx$ 95%) are pulled by the collector which is at high positive potential. The electrons are finally collected by the +ve terminal of battery V_{CB}, giving rise to collector current I_C.



- As soon as an electron from the emitter combines with a hole in the base region, an electron leaves the negative terminal of the battery V_{EB} and at the same time, the positive terminal of battery V_{EB} receives an electron from the base. This sets a base current I_B. Similarly, corresponding to each electron that goes from collector to positive terminal of V_{CB}, an electron enters the emitter from negative terminal of V_{EB}. Hence

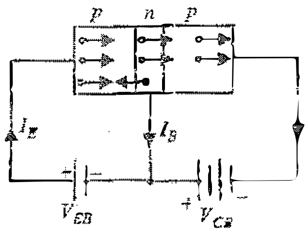
$$I_E = I_B + I_C \qquad [I_B << I_C]$$

Here I_B is a small fraction of I_C depending on the shape of transistor, thickness of base, doping levels, bias voltage, etc.



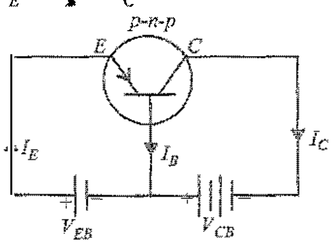
Action of *p-n-p* Transistor

- The forward bias of the emitter-base circuit repels the holes of emitter towards the base and electrons of base towards the emitter. As the base is very thin and lightly doped, most of the holes (≈ 95%) entering it pass on to collector while a very few of them (≈ 5%) recombine with the electrons of the base region.



- As soon as a hole combines with an electron, an electron from the negative terminal of the battery V_{EB} enters the base. This sets up a small base current I_B. Each hole entering the collector region combines with an electron from the negative terminal of the battery V_{CB} and gets neutralised. This creates collector current I_C. Both the base current I_B and collector current I_C combine to form emitter current I_E.

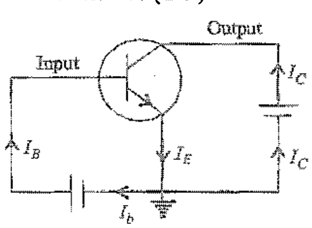
$\therefore\ I_E = I_B + I_C$



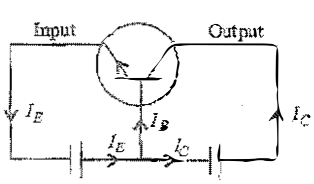
Basic Transistor Circuit Configurations

- In a transistor, only three terminals are available, viz., Emitter (*E*), Base (*B*) and Collector (*C*). Therefore in a circuit, the input/output connections have to be such that one of these (*E*, *B* or *C*) is common to both the input and the output. Accordingly, the transistor can be connected in either of the following three configurations:

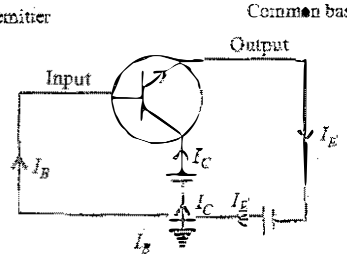
  Common Emitter (*CE*), Common Base (*CB*), Common Collector (*CC*).



Common emitter



Common base



Common collector

- **Common base current amplification 'α'**

  dc current gain is defined as ratio of output current I_C to the input current I_E.

$$\alpha_{dc} = \left[\frac{I_C}{I_E}\right]_{V_{CB}\ \text{constant}} \approx \left[\frac{0.95\, I_E}{I_E}\right] \approx 0.95$$

  Similarly, ac current gain is defined as the ratio of change in collector current to the change in emitter current.

$$\alpha_{ac} = \left[\frac{\Delta I_C}{\Delta I_E}\right]_{V_{CB}\ \text{constant}}$$

- **Common emitter current amplification 'β'**

  dc current gain is defined as ratio of output current I_C to the input current I_B.

$$\beta_{dc} = \left[\frac{I_C}{I_B}\right]_{V_{CE}\ \text{constant}} \approx \left[\frac{0.95\, I_E}{0.05 I_E}\right] \approx 19$$

  Similarly a.c. current gain is defined as the ratio of change in collector current to the change in base current.

$$\beta_{ac} = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE}\ \text{constant}}$$

- **Relation between α and β**

  We know

$$I_E = I_B + I_C$$

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

So, $\alpha = \dfrac{\beta}{1+\beta}$

$$\beta = \frac{\alpha}{1-\alpha}$$

Illustration 7

The current gain of a transistor in common emitter configuration is 70. If emitter current is 8.8 mA, then find

(i) base current.

(ii) collector current.

(iii) the current gain in common base configuration.

Soln.: Current gain, $\beta = \dfrac{I_C}{I_B}$, $I_E = I_B + I_C$

(i) $I_C = \beta I_B$ or $I_C = 70 I_B$ ...(i)

Since $I_E = I_B + I_C$ or $I_E = I_B + 70 I_B$

or $I_E = 71 I_B$

$\therefore\ I_B = \dfrac{I_E}{71} = \dfrac{8.8}{71} = 0.124$ mA

(ii) Collector current = I_C

$I_C = 70 I_B$ or $I_C = 70 \times 0.124 = 8.68$ mA

(iii) Current gain in common base configuration

$$\alpha = \frac{\beta}{1+\beta} \quad \text{or} \quad \alpha = \frac{70}{71} = 0.986$$

Input Characteristics of a Transistor

- The variation of the input current with the input voltage for a given output voltage is known as input characteristics of a transistor.

Output Characteristics of a Transistor

- The variation of the output current with the output voltage for a given input current is known as output characteristics of a transistor.

Transistor as a Switch

- When the transistor is used in the cut off region or saturation region, it acts as a switch.

Transistor as an Amplifier

- When the transistor is used in the active region, it acts as an amplifier.

Common Emitter Amplifier

- In the common emitter transistor amplifier, the input signal voltage and the output collector voltage are 180° out of phase.

dc Current Gain

- It is defined as the ratio of the collector current (I_C) to the base current (I_B).

$$\beta_{dc} = \frac{I_C}{I_B}$$

ac Current Gain

- It is defined as ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B).

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

Voltage Gain

- It is defined as the ratio of output voltage to the input voltage.

$$A_v = \frac{V_o}{V_i} = -\beta_{ac} \times \frac{R_o}{R_i}$$

where R_o and R_i are the output and input resistances. –ve sign represents that output voltage is opposite in phase with the input voltage.

Power Gain

- It is defined as the ratio of the output power to the input power.

$$A_p = \frac{\text{output power } (P_o)}{\text{input power } (P_i)}$$
$$= \beta_{ac} \times A_v$$

Note : Voltage gain (in dB) $= 20 \log_{10} \frac{V_o}{V_i}$

$$= 20 \log_{10} A_v$$

Power gain (in dB) $= 10 \log \frac{P_o}{P_i}$

Illustration 8

A transistor having $\alpha = 0.99$ is used in a common base amplifier. If the load resistance is 4.5 kΩ and the dynamic resistance of the emitter junction is 50 Ω, find

(i) voltage gain
(ii) power gain

Sol. (*i*) Voltage gain, $A_V = \frac{\alpha R_L}{R_e}$

or $A_V = \frac{0.99 \times 4500}{50} = 89.1$

(*ii*) Power gain = Current gain × Voltage gain

or $A_P = 0.99 \times 89.1$ or $A_P = 88.2$

LOGIC GATES

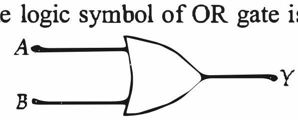
- A digital circuit with one or more input signals but only one output signal is known as logic gate.
- The logic gates are the building blocks of a digital system. Each logic gate follows a certain logical relationship between input and output voltage.
- There are three basic logic gates :
  - OR gate
  - AND gate
  - NOT gate

Truth Table

- It is a table that shows all possible input combinations and the corresponding output combinations for a logic gate.

OR gate

- An OR gate has two or more inputs but only one output.
- It is called OR gate because the output is high if any or all the inputs are high.
- The logic symbol of OR gate is



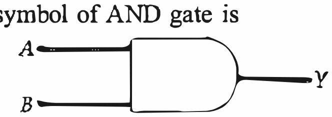
- The truth table for OR gate is

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

- The Boolean expression for OR gate is $Y = A + B$

AND gate

- An AND gate has two or more inputs but only one output.
- It is called AND gate because output is high only when all the inputs are high.
- The logic symbol of AND gate is



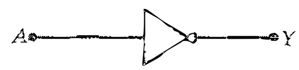
- The truth table for AND gate is

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

- The Boolean expression for AND gate is
  $Y = A \cdot B$

NOT gate

- The NOT gate is the simplest of all logic gates. It has only one input and one output.
- NOT gate is also called inverter because it inverts the input.
- The logic symbol of NOT gate is



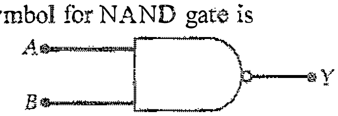
- The truth table for NOT gate is

Input	Output
A	Y
0	1
1	0

- The Boolean expression for NOT gate is
  $Y = \overline{A}$

NAND gate

- It is an AND gate followed by a NOT gate.
- The logic symbol for NAND gate is



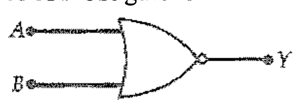
- The truth table for NAND gate is

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- The Boolean expression for NAND gate is
  $Y = \overline{A \cdot B}$

NOR gate

- It is an OR gate followed by a NOT gate.
- The logic symbol of NOR gate is



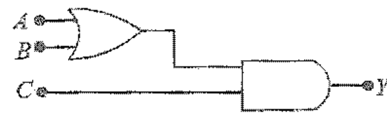
- The truth table for NOR gate is

	A	B	C
(i)	1	0	1
(ii)	0	1	1
(iii)	1	1	1

- The Boolean expression for NOR gate is
  $Y = \overline{A + B}$

Illustration 9

What must be the input to get an output $Y = 1$ from the circuit shown in figure?

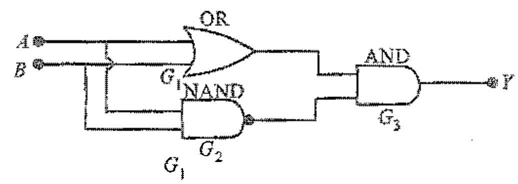


Soln.: It is a combination of OR and AND gate. There can be three schemes for getting output = 1.

	A	B	C
(i)	1	0	1
(ii)	0	1	1
(iii)	1	1	1

Illustration 10

The following configuration of gate is equivalent to which gate? Write its truth table.



Soln.: Output of $G_1 = A + B$

Output of $G_2 = \overline{A \cdot B}$

Output of $G_3 = (A + B) \cdot \overline{A \cdot B} = (A + B) \cdot (\overline{A} + \overline{B})$

$= A \cdot \overline{B} + \overline{A} \cdot B$

It represents XOR gate.

Truth Table		
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Illustration 11

Two inputs of NAND gates are shorted. What gate it is equivalent to?

Soln.: When two inputs of NAND gate are shorted, it is denoted by the Boolean expression $Y = \overline{A \cdot A} = \overline{A}$

It is, therefore, equivalent to NOT gate.